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Description

DYNAMIC RANDOM ACCESS MEMORY WITH SMART REFRESH SCHEDULER

BACKGROUND OF INVENTION

[0001] This invention relates to a Dynamic Random Access Memory (DRAM) devices, more particularly to logic technology based embedded DRAM devices.

[0002] As a solution to the problem of the manufacture of a System-on-Chip (SoC) type of device, use of an eDRAM device has numerous advantages over an embedded Static Random Access Memory (eSRAM). One of the biggest advantages of an eDRAM is the reduced area employed, roughly two to three times less than the area required by an eSRAM. However, the advantage of eDRAMs is diluted by the process complexity and the additional cost caused by the unique process of manufacturing DRAM devices. Therefore, both simplification of the manufacturing process and reduction of the cost of the manufacturing process are required concomitantly maintaining reduced area

advantages. Use of logic technology based eDRAMs is such an example. Except for the process of capacitor fabrication, the processing is almost the same as for the logic process. Therefore, a relatively low threshold Cell Access Transistor (CAT) results in improvement of performance and removal of an additional mask step. But, a low threshold CAT will bring about a severe data retention problem because of its high leakage current. To compensate for data leakage, a more frequent data refresh operation is needed. More frequent data refresh operation gives rise to another performance degradation to system reducing memory availability.

SUMMARY OF INVENTION

[0003] To avoid or reduce data retention related issues, in accordance with this invention, a technique is provided and implemented. In some DRAMs, like SRAMs, the refresh operation is not seen by the user or the system while the refresh is being done internally. However, there is conflict between the normal DRAM access and the internal refresh. To manage this conflict, an intelligent scheduler is needed and in accordance with this invention, such a scheduler is provided.

[0004] An object of this invention is to provide a refresh sched-

uler book unit to manage the internal refresh operation of a DRAM memory without creating a conflict between the internal refresh function and the normal access function.

[0005] It is another object of this invention to provide an efficient refresh schedule algorithm that arbitrates the conflict between normal operation and internal refresh operation. It is also another object to implement the scheduling scheme for managing refresh operation by using the search algorithm that simplifies the circuit implementation and minimizes a penalty from scheduling.

[0006] This invention provides a smart refresh scheduler book unit that can handle or coordinate internal refresh operation and normal access operation. By doing so, the greater frequency of refresh operations caused by a leaky logic cell transistor can be hidden or invisible to the system. It greatly improves memory availability while using a very leaky cell device. The scheduler keeps the refresh status of each memory bank or array by using up/down shift registers and decides which bank to be refreshed. The search operation of this invention is fast and easy to implement.

[0007] The refresh bank search algorithm in this invention is feasible to implement and enables simple circuit implemen-

tation while minimizing the penalty caused by a refresh bank search operation.

[0008] In accordance with this invention a DRAM, which includes a plurality of memory banks (i.e. banks or arrays), there is a pair of separate flag bit registers for each bank with the flag bit registers that are shifted up/down respectively. A comparator for each bank provides a comparator output. An arbiter for each bank is connected to receive a flag bit up signal and a flag bit down signal from the flag bit registers for that bank and the comparator output from the comparator for that bank. The arbiters are connected to receive a conflict in signal and to provide a conflict out signal. The pair of flag bit registers represent a refresh status of each bank and designate memory banks or arrays that are ready for a refresh operation.

[0009] In accordance with another aspect of this invention, a dynamic random access memory (DRAM) with a plurality of memory banks (i.e. banks or arrays) including a refresh scheduler book unit is provided. The DRAM includes a pair of separate flag bit registers for each bank with the flag bit registers being shifted up/down respectively, a comparator for each bank which provides a comparator output, an arbiter for each bank connected to receive a flag

bit up signal and a flag bit down signal from the flag bit registers for that bank and the comparator output from the comparator for that bank, the arbiters being connected to receive a conflict in signal and to provide a conflict out signal, and the pair of flag bit registers representing a refresh status of each bank and designating memory banks or arrays that are ready for a refresh operation, memory access sequencing means for providing a sequence of refresh operations, and a conflict signal generator included in each of said arbiters. Preferably, the DRAM includes an arbiter which coordinates refresh bank activation by combining comparator results and refresh bank activation priority schedule; and a row address counter (RAC) for each bank keeps the refresh history of each bank and generates a row address to be refreshed. Preferably, components comprising the refresh scheduler book unit are isolated from each bank and the refresh scheduler book unit sends to each bank both of a selected refresh bank address and refresh row address kept by row address counter. Preferably, all components except row address counter (RAC) are isolated from each bank or array and send to each bank or array a selected refresh bank address.

Brief Description of Drawings

[0010] The foregoing and other aspects and advantages of this invention are explained and described below with reference to the accompanying drawings, in which:

[0011] FIG. 1 shows a multi-bank or multi-array memory with four memory banks to illustrate the basic concept of this invention.

[0012] FIGS. 2A and 2B show block diagrams of key components of a system in accordance with this invention.

[0013] FIG. 3 shows the details of Row ADD MUX of FIG. 2 and Row Address Counter (RAC) and its connection to the Word Line Driver in accordance with this invention.

[0014] FIG. 4 shows the details of the structure of the comparator blocks shown in FIGS. 2A and 2B in accordance with this invention.

[0015] FIG. 5 shows the connections to a generic arbiter in accordance with this invention.

[0016] FIGS. 6A-6C show how the flag bits are changed in accordance with this invention.

[0017] FIG. 6D shows a hybrid form of flowchart of an algorithm, signal, and devices, in accordance with the invention and FIGS. 6A-6C.

[0018] FIG. 7 shows an alternative to the embodiment of FIG. 2B

that is similar to FIG. 1.

[0019] FIG. 8 shows an alternative of the embodiment of FIG. 5.

[0020] FIG. 9A shows a circuit diagram embodying the generic arbiter of FIG. 5.

[0021] FIG. 9B shows a conflict signal generator which is a component of the arbiter of FIG. 9A formed by a CMOS pair of PMOS and NMOS transistors. A "conflict out" signal is received at the gate electrode of the NMOS transistor from any one of the arbiters of the banks of the DRAM memory and a global "conflict in" signal is provided as the output at the source/drain node between the PMOS and NMOS transistors of the CMOS pair.

DETAILED DESCRIPTION

[0022] FIG. 1 shows a multi-bank or multi-array memory with four memory banks 19A-19D to illustrate the basic concept of this invention. In a multi-bank or multi-array memory with several banks 19A-19D in each cycle, only one bank or array is activated for the purpose of normal memory access while one or more of the other banks are activated for the purpose of being refreshed. Therefore, during each cycle, more than one bank or array is activated simultaneously. In FIG. 1 where two banks 19A/19C

are activated at the same time, the first bank 19A is accessed for a normal read or a normal write operation, while a second bank 19C is refreshed. The decision as to whether or not a particular bank will be refreshed is done by are fresh scheduler book unit 13. The refresh scheduler book unit 13 manages the refresh schedule of every bank 19A, 19B, 19C and 19D or memory array and issues the global address on lines 14 (RBA, RRA) for a refresh operation while simultaneously bypassing normal access bank address lines including BA lines 16A and RA lines 16B issued externally by the user or system to row decoders 15A, 15B, 15C and 15D. On the one hand, lines 14B carry the RBA (Refresh Bank Address) signal and lines 16A carries the BA (Bank Address)signal respectively. Also, lines 14A carry the RBA (Refresh Bank Address) signal and lines 16B carry the RA (Row Address) signal. The refresh scheduler book unit 13 sends mode selection (mode SEL) signals on lines 11 together with the refresh address RA signals on lines 16B to the row decoders 15A to 15D. The mode selection signal lines 11 carry the information as to which address the row decoder 15A/15B/15C/15D of the selected bank 19A/19B/19C/19D should accept.

[0023] The role of the refresh scheduler book unit 13 is to arbi-

trate the possible conflicts between the incoming normal access address, and to decide which bank to refresh and track the refresh status of each bank.

[0024] FIGS. 2A and 2B show block diagrams of key components of the system of this invention. FIG. 2A shows the connections for a single generic bank 19. In FIG. 2A, an address buffer 17 supplies the BA signals on lines 16A and the RA signals on lines 16B. A refresh scheduler book unit 13 in accordance with this invention comprises a Row ADDress MUltipleXer (Row ADD MUX) 23, up flag register FBU 21 and down flag register FBD 22, comparator block 24 and arbiter 25. A row address decoder 27, a wordline driver 28 and a Bank n-119Z are also shown.

[0025] FIG. 2A shows a single block connection. FIG. 2B shows all connections among multiple banks, illustrating a preferred embodiment of this invention.

[0026] A Fixed Refresh Bank Address register (Fixed RBA) 29 is a uniquely assigned bank address to the shown bank through an output line 14A connected to both the comparator block 24 and the Row ADD MUX 23.

[0027] FIG. 4 shows the details of the structure of one of the comparator blocks 24 shown in FIGS. 2A and 2B. Each comparator block 24 receives two compare inputs, the in-

coming bank address from BA line 16A and the fixed bank address from RBA line 14A and two control inputs, FBU input 41 from FBU register 21 and FBD input 42 from FBD register 22. For each comparator block 24, the respective FBU register 21 and the respective FBD register 22 are connected to that comparator 24 and the corresponding arbiter 25. The FBU register 21 and the FBD register 22 each have a bit shifting capability. The actual connections of FBU register 21 and FBD register 22 are clearly shown in FIG. 2B and FIG. 4. All of FBUs in FIG. 2B are serially connected and shift the bit information of each FBU register 21 downwardly. Also, all of FBD registers 22 are serially connected and shift the bit information of each FBD register 22 upwardly.

[0028] The arbiter 25 also supplies Mode Select Signal on line 26 to the Row Add MUX 23 as shown in more detail in FIGS. 6 and 3.

[0029] A conflict signal line 62 is connected to send and receive conflict signals to and from the arbiter 25.

[0030] The BA signal on lines 16A is supplied to comparator block 24 and row address multiplexer 23. The RA signal on lines 16B is supplied to the row address multiplexer 23 only.

[0031] FIG. 2B shows three sets of circuits for a few exemplary banks BANK0 19X, BANK32 19Y, and bank BANKn-1 19Z out of n banks in an array thereof connected to lines 16A/16B and 62 as in FIG. 2A.

[0032] FIG. 3 shows the details of Row ADD MUX 23 of FIG. 2 and Row Address Counter (RAC) 31 and its connection to the Word Line Driver 28. It is comprised of RAC (Row Address Counter) counter 31 and two multiplexers comprising upper MUX 32 and lower MUX 33. Both upper MUX 32 and lower MUX 33 in FIG. 3 have a common input select signal, which is the selection signal, i.e. the Mode SEL signal on line 26 from the arbiter 25 as shown in FIGS. 2A, 2B and 6. The upper MUX 32 in FIG. 3 selects one out of two row address inputs, one on line 31 from RAC counter 31 and the other on RA line 16B from the address buffer 17 in FIGS. 2A and 2B. The RAC counter 31 provides the row address to be refreshed within each bank and automatically increases the row address therein after the selected bank is refreshed. The role of RAC 31 is to keep track of the refreshing process progressing from bank to bank by increasing the count in the respective RAC counter 31 whenever the bank is refreshed. The lower MUX 33 selects one bank address out of two bank address inputs, includ-

ing BA input on lines 16A and RBA inputs on line 14A. The two MUX units 32/33 select the refresh address or normal address depending on the Mode SEL signal polarity on line 26 from the refresh scheduler book unit 13.

[0033] The Mode SEL signal on line 26 determines whether a bank will be normally accessed or refreshed. If the incoming bank address on line 16A and the refresh bank address on RBA line 14A are the same, the Mode SEL signal on line 26 selects the incoming bank address (BA) on line 16A and row address (RA) on line 16B and the bank performs its Normal operation. On the other hand, if the incoming bank address (BA) on line 16A and the refresh bank address on line 14A are not the same and the decision to refresh the bank is made, the Mode SEL selects the refresh bank address (RBA) on line 14A and RAC counter output to row decoder.

[0034] The flag registers FBU 21, FBD 22 of each bank indicate whether that bank is a candidate for a refresh operation. During every cycle, one FBU bit and one FBD bit have a valid flag bit. Accordingly, two banks are always candidates for a refresh operation. The comparator 43 in each bank which has a valid flag bit compares the incoming bank address for normal access with Fixed Refresh Bank

Address. (Fixed RBA) on line 14B.

[0035] The comparator 43 in comparator block 24 in FIG. 4 compares the incoming bank address BA on line 16A that has passed through address buffer 17 in FIGS. 2A and 2Bwith the bank address of a candidate bank to be refreshed, i.e. the Fixed RBA on line 14B. If the two bank addresses are the same, it means the candidate bank is going to be accessed for normal read or write. Otherwise, the candidate bank can be refreshed. The output signal from the comparator 43 is sent on line 44 to the arbiter 25 and used to decide which bank is to be refreshed.

[0036] Referring again to FIG. 4, in more detail, the comparator block 24 of each bank is connected to the incoming bank address (BA) on line 16A, Fixed Refresh Bank Address (Fixed RBA) line 14B, FBU line 41 and FBD line 42. The FBU line 41 and FBD line 42 are connected to an Exclusive OR gate (XOR) 46. When the two flag bits are different, the comparator 43 can be enabled to generate a comparison result by the XOR 46 providing a high output online 47, but otherwise comparator 43 will be disabled because of a low input on line 47. In other words, a bank that has two valid different flag bits can be a candidate for a refresh operation. The flag registers of each bank are two bit reg-

isters, and each bit is connected serially with adjacent banks comprising shift register in up/down direction respectively. The flag bits are shifted or kept as every refresh operation is done.

[0037] FIG. 5 shows the connections to a generic arbiter 25. The arbiter 25 is connected to receive FBU and FBD bits on line 41 and 42 in each bank, comparator result on line 44 and conflict signal on common line 62. The arbiter 25 generates Mode SEL and conflict signal as outputs. The conflict signal on line 62 behaves as both an input and an output depending on flag bits. The arbiter 25 of a bank that has FBU "0" and FBD "1" will not take the conflict signal on line 62 as an input and instead bypass the comparator result on line 44 to conflict signal line 62. On the other hand, the arbiter 25 of the bank that has FBU "1" and FBD "0" will take the conflict signal on line 62 as an input without bypassing the comparator result from line 44 to the conflict signal line 62.

[0038] FIGS. 6A-6C show how the flag bits are changed. FIG. 6A shows the initial condition of the flag bits. FBU of bank n-1 and FBD of bank 0 are set to "1" and the rest of FBU and FBD are set to "0". This means that two banks, "n-1" bank 19Z and "0" bank 19X in FIG. 2B, are candidates for re-

fresh operations. A selected "n-1" bank 19Z or "0" bank 19X is to be refreshed and the corresponding FBU or FBD bit is shifted by one bit. If the "n-1" bank 19Z were refreshed, FBU "1" at If "n-1" bank 19Z is shifted to bank n-2 as shown in FIG. 6B.

[0039] FIG. 6C shows another situation where "'0" bank 19X is refreshed and FBD "1" of "0" bank 19X is shifted to bank 1(not shown).

[0040] In this invention, referring to FIG. 6A, 6B and 6C refresh bank selection is done by a binary search. Initially, two banks, the uppermost one of FBU in FIG. 6A and bottom one of FBD in FIG. 6A, have flag bit "1". There are some different scenarios depending on incoming bank address and refresh bank selection priority. First, if the incoming bank address matches one of two bank addresses, the unmatched bank is selected for refresh. Simultaneously, the flag bit "1" of the selected bank is shifted downward or upward while the flag bit "1" of the unselected bank is being kept at the same place. Second, if the incoming address does not match with two refresh candidate bank addresses, the bank that has the refresh bank selection priority determined by arbiter 25 will be selected and shift the flag bit "1". This refresh bank selection operation will

be continued until all of the banks are refreshed.

[0041] FIG. 6D shows a hybrid form of flowchart of an algorithm, signal, and devices, in accordance with the invention and FIGS. 6A-6C, which operates as follows:

[0042] 1. At the start 72 of the algorithm, the program proceeds along line 73 to block 74 to perform a memory access sequence, wherein all of the flag bit registers FBU 21 and FBD 22 are reset as follows:

[0043] FBU(n-1)=FBD(0)=1;

[0044] FBU(n-2),..= FBU(0).= FBD(1)...FBD(n-1)=0;

[0045] All FBUs and FBDs except FBU(n-1) and FBD(0) are reset to "0".

[0046] 2. The output of reset block 74 on line 75 flows to comparator block(i) 24i, comparator block 24j, arbiter(i) 25i and arbiter(j) 25j.

[0047] The bank j flag bit information is FBU(j)=0, FBD(j)=1, enables comparator block(j) 24j and compares the incoming Normal access bank (BA) address on line 18A with the fixed refresh bank Address (RBA) on line 14A as explained above in connection with FIG. 4. The result (output) which is a YES/NO signal on line 44j from comparator block(i) 24j is input to Arbiter(j) 25j.

[0048] 3. The arbiter(j) 25j is also enabled by the input signal combinations, FBU(j)=0 and FBD(j)=1on line 75 from step 74 in the program and receives the comparator output j on line 44j and generates a conflict signal on line 62j as an output from the arbiter 25j which is supplied as an input to the arbiter 25i. Arbiter 25i provides a mode select (i) output on line 26i and arbiter 25j provides a mode select output on line 26j as explained in connection with generic arbiter 26 in FIG. 6. If the output from comparator block 24j is "YES", the mode select j signal transmitted on line 26j is "1" which shifts FBD(0)...(n-1) by 1 bit upward from LSB to MSB on line 75j to line 75.

[0049] If the output from comparator block 24j is "NO", the conflict signal is "1" and sent on line 62j to bank i as an input to Arbiter 25i.

[0050] This keeps the Mode select j on shift line 26j to the FBD(j) at "0" on line 75j to line 75 and does not change the register pattern FBD(0)...(n-1).

[0051] 4. Arbiter(i) 25i is enabled by the input signal combinations, FBU(i)=1 and FBD(i)=0 on line 75 and receives an output from comparator block(i) 24i on line 44i and the conflict signal from arbiter(j) 25j on line 62j as inputs.

[0052] If the output from comparator block(i) 24i on line 44i i is

"YES" and the conflict signal on line 62j is "1", the Mode select(i) output on line 26i is "1" which is a shift signal into FBU(n-1)...FBU(0) by 1 bit downward from MSB to LSB.

[0053] If the output of comparator block 24 i is "NO", then the Mode select(i) value on line 26i is "0".

[0054] 5. The mode select signals i and j on lines 26i and 26j are inputs to ROW ADD MUX blocks 23i and 23j as indicated by generic ROW ADD MUX 23 shown in FIG. 3 and the selected addresses will fire corresponding word lines.

[0055] 6. In the next cycle, the shifted or non-shifted FBU and FBD values on lines 75i and 75j are inputs to the comparator blocks 24i, 24j and the arbiters 25i, 25j.

[0056] Following the bank selection algorithm above, in multiple n banks, any 1 out of n (1/n) bank is busy for normal access but n-1out of n banks(n-1/n) are idle for refresh at first cycle. Next cycle, 1/n bank is busy but n-2 out of n-1 (n-2/n-1) is idle for refresh. At n-1 cycle, any 1/n bank is busy and 1 out of 2 is idle for refresh. Finally, only one bank is not refreshed yet after n-1 cycles. The refresh scheduler book unit 13 handles memory bank selection effectively while reducing complexity from the refresh scheduler book unit 13.

[0057] The arbiter 205 mediates the conflict between two candi-

date banks and decides which bank to be refreshed. The arbitration is done through two flag bit information and common conflict signal. The comparator results of two candidate banks are shared through arbiters 25 connected to receive common conflict signals on line 62. When two candidate banks are available for a refresh operation, one of two banks is selected through arbitration following the given priority. In accordance with this invention, the priority is given to the bottom side bank. The "bottom side" refers to the bank FBD(j)=1 and FBU(j) =0, i.e. searched from bank "0". The "upper side" refers to the bank that has FBD(j)=0 and FBU(j) =0, i.e. searched from bank "n-1".

[0058] In FIG. 2B, all of the key components of the refresh scheduler book unit 13 are distributed to each bank i, j, etc. Only the communication channels, such as conflict signal and bank address are distributed over all memory banks.

[0059] FIG. 7 shows an alternative to the embodiment of FIG. 2B that is similar to FIG. 1. All of the key components of the refresh scheduler book unit 713 in FIG. 2 except Row Address MUX 23 are collected into one place in the refresh scheduler book unit 713 and only a selected refresh bank address 714B is sent to each bank 19X, 19Y and 19Z to-

gether with access bank address on line 716A.

[0060] FIG. 8 shows an alternative of the embodiment of FIG.2B. All of the key components of the refresh scheduler book unit 813 in FIG.2 including RAC 31 are collected into one place in the refresh scheduler book unit 813 and the selected refresh bank address814A and refresh row address 814B are sent to each bank 19X, 19Y and 19Z together with normal address 816B and bank address on line 816A.

[0061] FIG. 9A shows a circuit diagram embodying the arbiter 25i of FIG. 6D for bank (i) of the DRAM memory device of this invention.

[0062] FIG. 9B shows a conflict signal generator162 which is a component of each generic arbiter 25 of FIGS. 5 and 9A (separate from the arbiter 25 of FIG. 9A for convenience of illustration) comprising a CMOS pair of PMOS and NMOS transistors P1/N1. A "conflict out" signal is received on line 62OUT (from any one of the arbiters of the DRAM memory)at the gate electrode of the NMOS transistor N1 of arbiter 25i of FIG. 6D from an arbiter 25j in FIG. 6D of the previous bank "j".

[0063] A global "conflict in" signal is provided at the common drain node on line 62IN as the output between the PMOS and NMOS transistors of the CMOS pair to be supplied to

the next lowest arbiter 25h which is not shown in FIG. 6D. The source of PMOS transistor P1 is connected to power supply voltage Vdd. The source of NMOS transistor N1 and the gate of PMOS transistor P1 are connected to ground.

[0064] Referring to FIG. 9A, FBU(i) and FBD(i) on lines 41 and 42 are from the flag bit registers of each bank. The comparator(i) input on line 44i is the comparator result of each bank.

[0065] FBD(i) and inverted FBU(i) from inverter IN1 are inputs to 2 input NAND gate NA3 which is inverted by inverter IN7. The output of inverter IN7 together with comparator result(i) on line 44i generate an output inverted by inverter IN8 which produces a conflict output(i) on line 62OUT.

[0066] The conflict output(i) signal on line 62OUT and the output of NAND gate NA3 which has been inverted twice by inverters IN7 and IN9 are inputs to NOR gate NOR2 and decides whether Mode SEL(i) is "0" or "1".

[0067] On the other hand, FBU(i) and inverted FBD(i) via inverter IN6 are inputs to 2 input NANDGate NA1. The output of IN2, comparator result(i) and the "conflict in" line 62 IN are input to NOR gate NOR1 and the output of NOR1 which passes through NAND NA5 decides the Mode SE-

LECT(i) output on line 26i.

[0068] Referring to FIG. 9B, the conflict out(i) signal on line 62OUT from inverter IN8 is connected to the gate of NFET N1 and generates the "conflict in" signal on line 62IN in FIGS. 9A and 9B which is a global signal and input to 3 input NOR NOR1.

[0069] The functions of the circuits of FIGS. 9A and 9B are as follows:

[0070] FBU(i)="0";

[0071] FBD(i)="1";

[0072] Comparator(i)="1": generates conflict out "1" and keep Mode SEL "0" selecting the normal access address;

[0073] FBU(i)="0";

[0074] FBD(i)="1";

[0075] Comparator(i)="0": keeps conflict out "0" and sets Mode SEL "1" selecting the refresh address.

[0076] FBU(i)="1";

[0077] FBD(i)="0";

[0078] Comparator(i)="0".

[0079] 1) if conflict in is low, sets Mode SEL "1" selecting refresh address.

[0080] 2) if conflict in is high, keeps Mode SEL "0" selecting the normal access address;

[0081] FBU(i)="1";

[0082] FBD(i)="0";

[0083] Comparator(i)="1": keeps Mode SEL "0" selecting the normal access address.

[0084] FBU(i)="0";

[0085] FBD(i)="0";

[0086] Comparator(i)="1", or "0": Regardless of comparator result, Mode SEL is "0" selecting the normal access address.

[0087] Many alternatives can be possible in terms of placement of each key component. Accordingly, the present invention is intended to embrace all such alternatives as fall within the following claims.

[0088] Having thus described the invention, what is claimed as new and desirable to be secured by Letters Patent is as follows.